Amendment to the Claims

Please amend the Claims as follows and without prejudice. This listing of Claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (CURRENTLY AMENDED) A method of creating an operational integrated circuit, comprising:
    a. creating a first block comprising a [[PHEMT]] pHEMT enhancement mode transistor on a substrate;
    b. creating a second block comprising a [[PHEMT]] pHEMT depletion mode transistor on the substrate, the second block operatively connected to the first block; and
    c. creating a third block comprising a power pHEMT transistor on the substrate, the third block operatively connected to at least one of the first block and the second block.
2. (ORIGINAL) A method according to claim 1 wherein the operational integrated circuit is created in a single fabrication process.
3. (ORIGINAL) An integrated circuit, comprising:
    a. a first block comprising an enhancement mode pHEMT transistor on a substrate;
    b. a second block comprising a depletion mode pHEMT transistor on the substrate, the second block operatively connected to the first block; and

c. a third block comprising a power pHEMT transistor on the substrate, the third block operatively connected to at least one of the first block and the second block.

4. (PREVIOUSLY PRESENTED) An integrated circuit according to claim 3 further comprising:

a. an analog input for electrical signals in communication with at least one of the first block, the second block, and the third block;

b. a clock input in communication with at least one of the first block, the second block, and the third block; and

c. a digital output for electrical signals in communication with at least one of the first block, the second block, and the third block;

d. wherein the first block, the second block, and the third block connect to form an analog to digital converter.

5. (ORIGINAL) An integrated circuit according to claim 3 wherein the integrated circuit is a microwave and millimeter wave integrated circuit (MMIC).

6. (PREVIOUSLY PRESENTED) An integrated circuit according to claim 3 wherein the circuit is capable of operating at a frequency within the range of from very low frequency up to and including X-band frequencies.

7. (ORIGINAL) An analog to digital converter, comprising an enhancement mode pHEMT device, a depletion mode pHEMT device, and a power pHEMT device on a single substrate.

8. (PREVIOUSLY PRESENTED) An analog to digital converter according to claim 7, wherein the substrate comprises a group III-V material.

9. (ORIGINAL) An analog to digital converter according to claim 8, wherein the substrate comprises gallium arsenide.

10. (ORIGINAL) A plurality of integrated circuits on a single substrate, the plurality of integrated circuits adapted to be interconnected to form a functional block, at least one of the plurality of integrated circuits comprising:

    a. a first block, comprising an enhancement mode pHEMT transistor on a substrate;

    b. a second block, comprising a depletion mode pHEMT transistor on the substrate, the second block operatively connected to the first block; and

    c. a third block, comprising a power pHEMT transistor on the substrate, the third block operatively connected to at least one of the first block and the second block.

11. (ORIGINAL) A plurality of integrated circuits on a single substrate according to claim 10 wherein the plurality of integrated circuits can be interconnected to form a plurality of functional blocks which can be interconnected to create an operational electronic device.

12. (PREVIOUSLY PRESENTED) An integrated circuit according to claim 3, wherein each of said pHEMT transistors comprises a recess defined in said substrate and a gate formed in said recess.

13. (PREVIOUSLY PRESENTED) An integrated circuit according to claim 12, wherein the recess of the depletion mode pHEMT transistor is a single recess.

14. (PREVIOUSLY PRESENTED) An integrated circuit according to claim 12, wherein the recess of the power pHEMT transistor is a double recess.

15. (PREVIOUSLY PRESENTED) An integrated circuit according to claim 12, wherein the recess of the enhancement mode pHEMT transistor is a single recess.

16. (PREVIOUSLY PRESENTED) An integrated circuit according to claim 15, wherein the recess of the power pHEMT transistor is a double recess, the recess of the depletion mode pHEMT transistor is a single recess, and each of said recesses is defined through at least one common layer of said substrate.

17. (PREVIOUSLY PRESENTED) An integrated circuit according to claim 12, wherein at least one of said gates is a T-gate.

18. (PREVIOUSLY PRESENTED) An integrated circuit according to claim 3, wherein a pinch off voltage of the depletion-mode pHEMT transistor is about positive 0.1 volts.

19. (PREVIOUSLY PRESENTED) An integrated circuit according to claim 3, wherein a pinch off voltage of the enhancement-mode pHEMT transistor is about negative 1.0 volts.